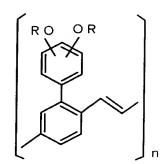
Chem. 1



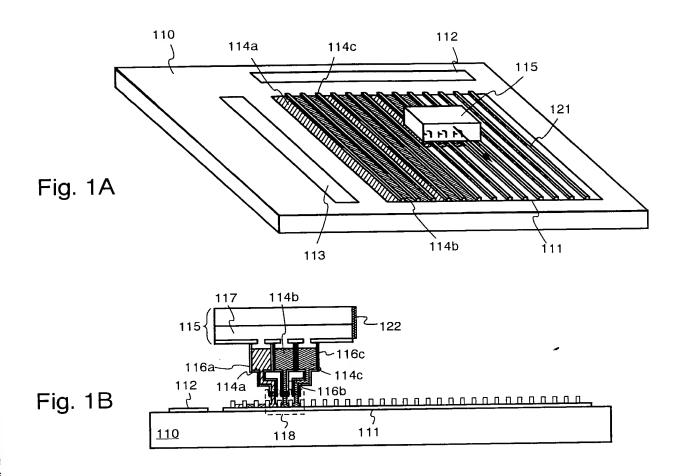
Chem. 2

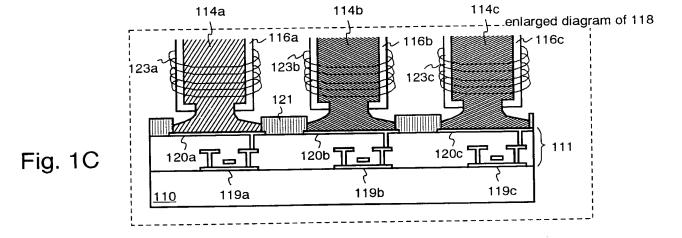
Chem. 3

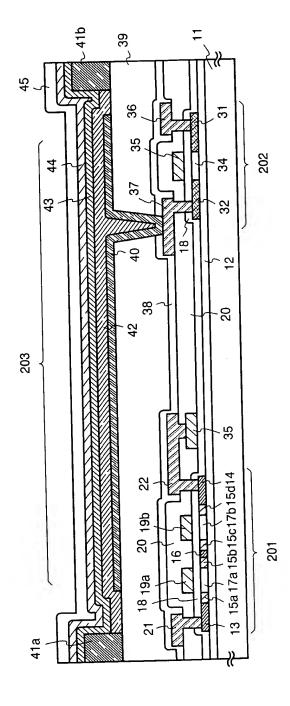
$$CH=CH$$

Chem. 4

Chem. 5







23:gate electrode 31:source region 32:drain region 34:channel forming region 35:gate electrode 36:source wiring 37:drain wiring 38:first passivation film 39:second interlayer insulating film 40:pixel electrode(anode) 41:bank 42:EL layer 43:cathode 44:protecting electrode 16:high concentration impurity region 17a,17b:channel forming region 18:gate insulating film 19a,19b:gate electrode 20:first interlayer insulating film 21:source wiring 22:drain wiring 11:substrate 12:base film 13:source region 14:drain region 15a-15d:LDD region 45:second passivation film

Fig. 2

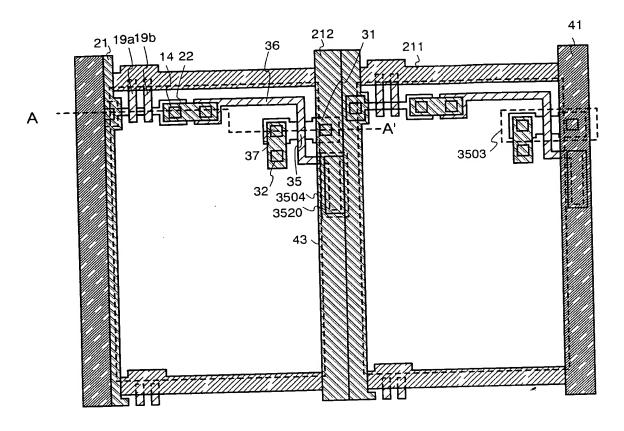


Fig. 3A

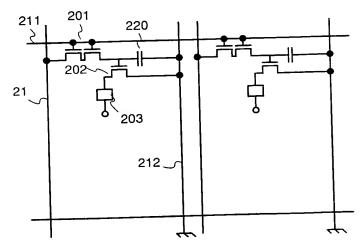
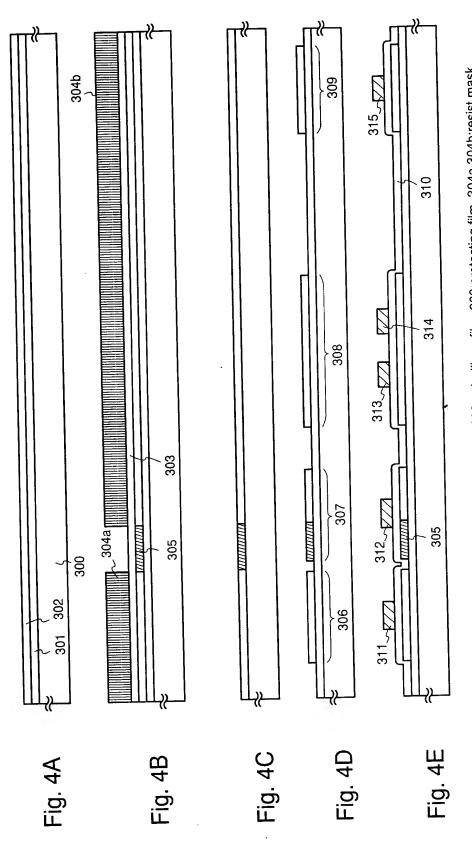
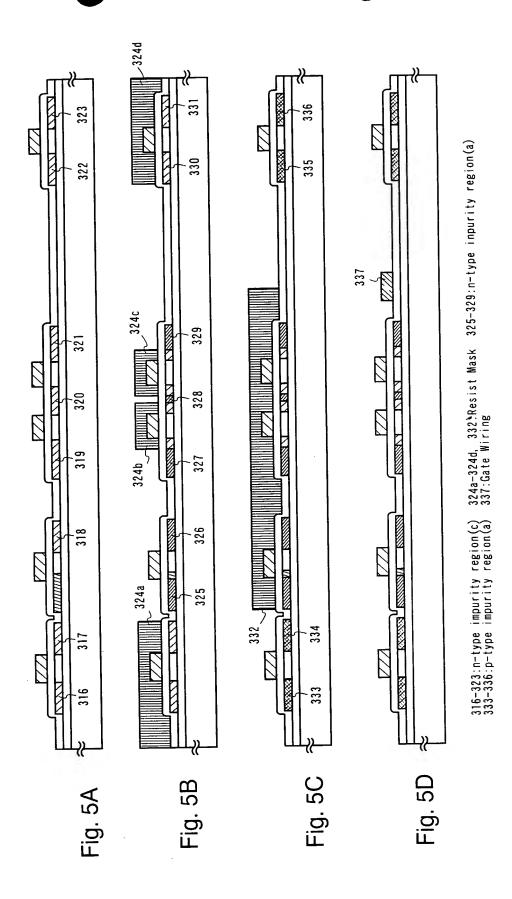
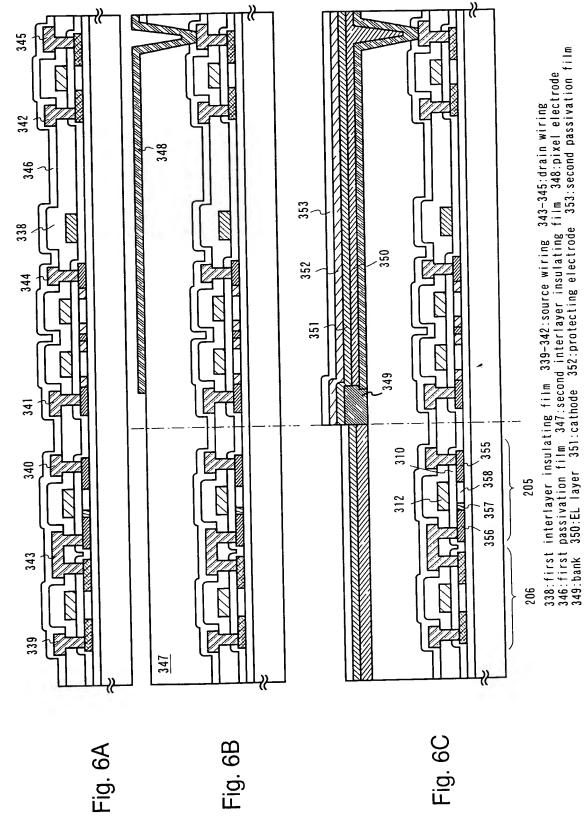


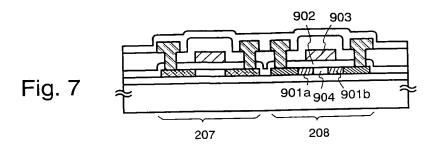
Fig. 3B

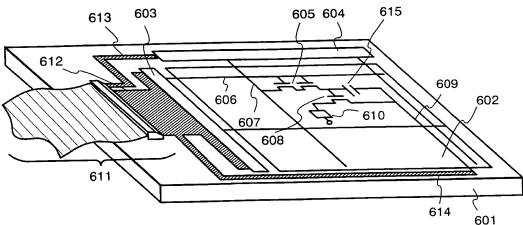


300:glass substrate 301:base film 302:polysilicon film 303:protecting film 304a,304b:resist mask 305:n-type impurity region 306-309:active layer 310:gate insulating film 311-315:gate electrode









601:substrate 602:pixel portion 603:gate side driver circuit 604:source side driver circuit 605:switching TFT 606:gate wiring 607:source wiring 608:current control TFT 609:electric power supply 610:EL element 611:FPC 612-514:input/output terminal 615:capacitor

Fig. 8

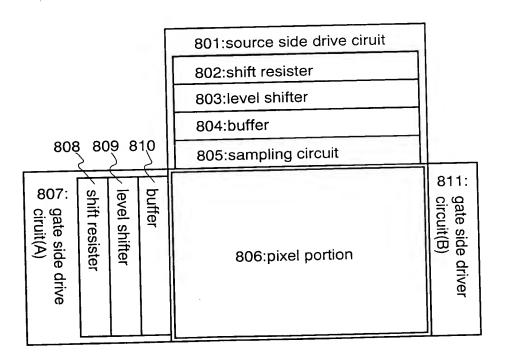
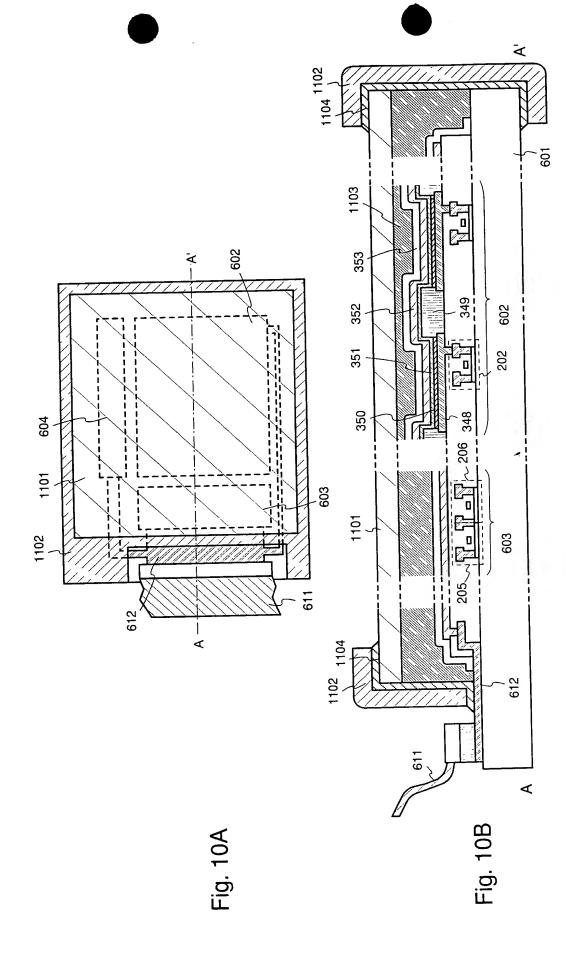
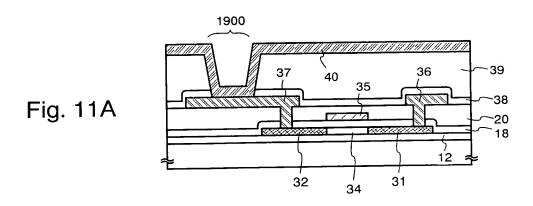
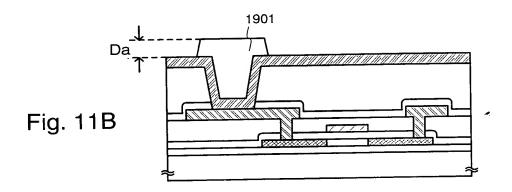
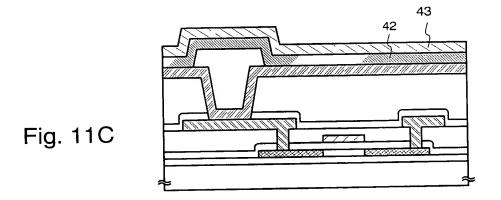


Fig. 9









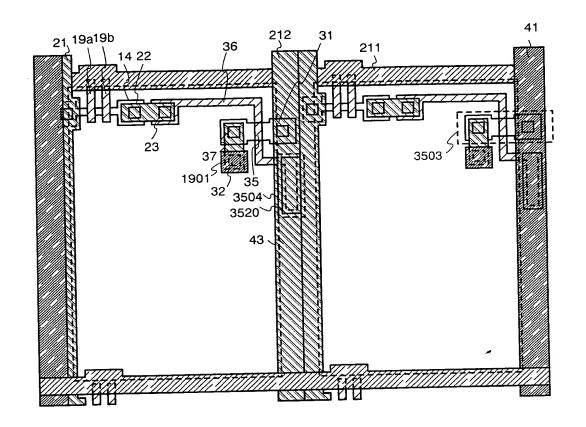
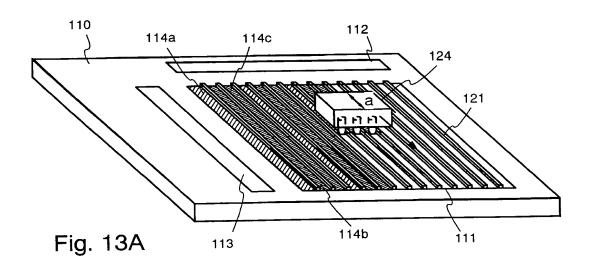


Fig. 12



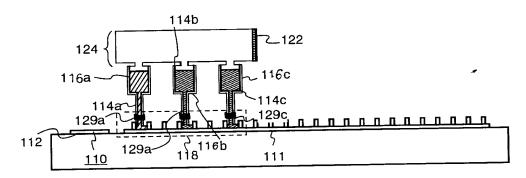


Fig. 13B

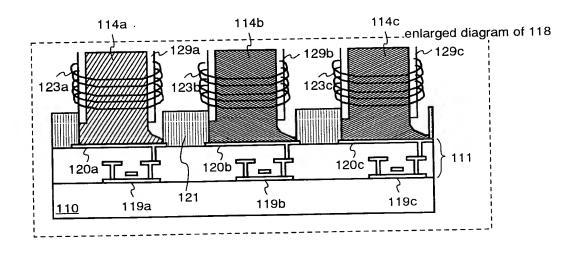


Fig. 13C

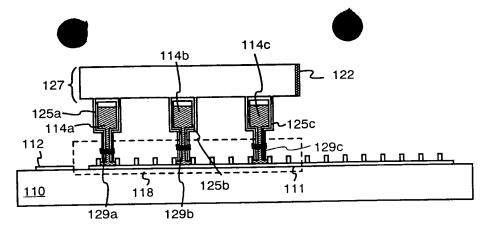


Fig. 14A

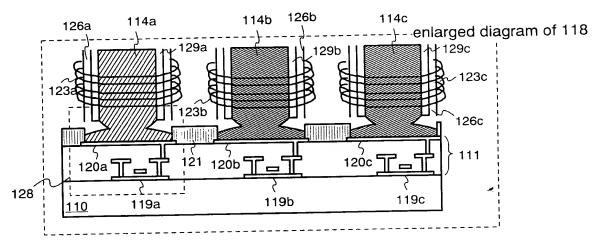


Fig. 14B

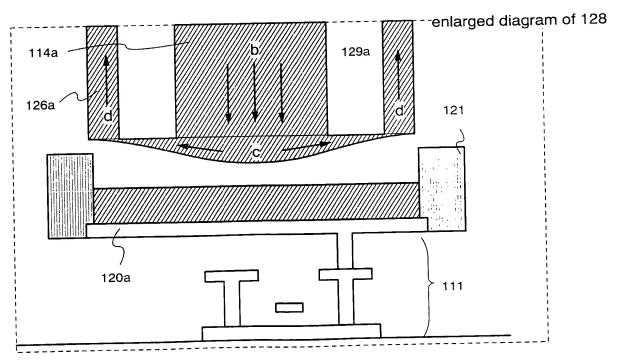
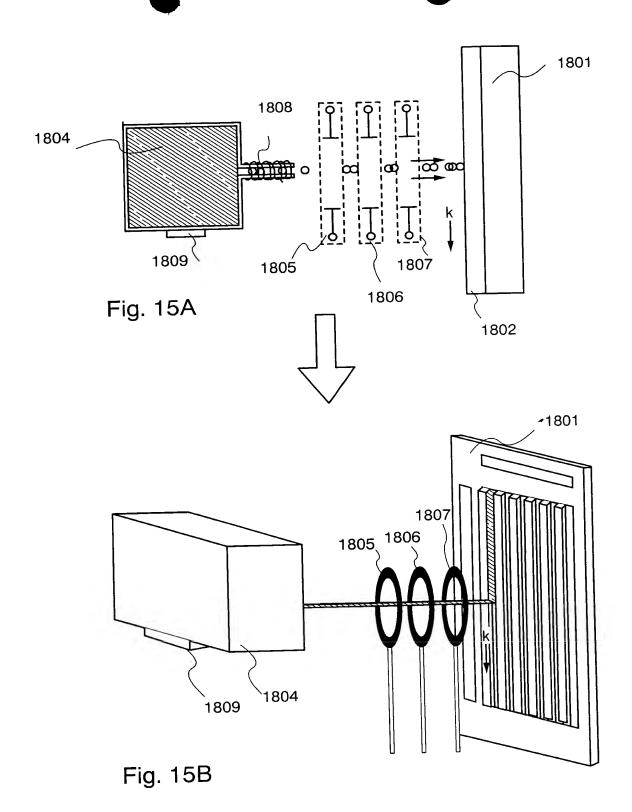
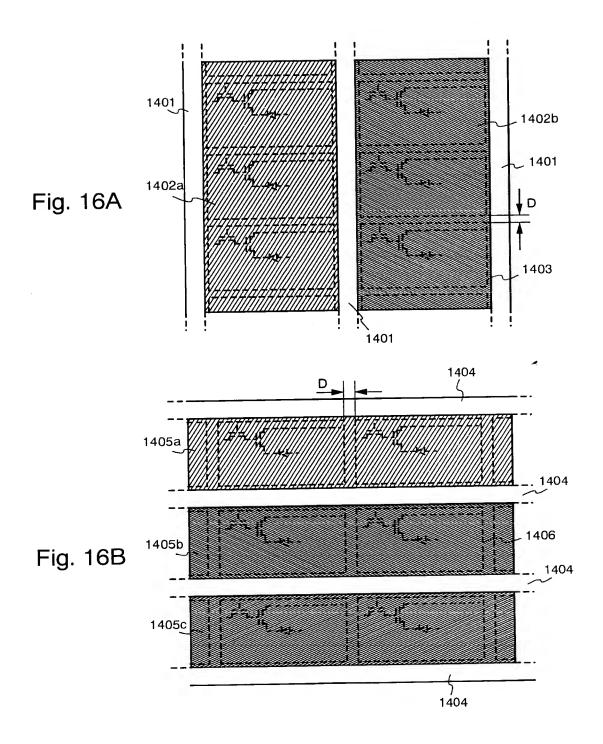


Fig. 14C





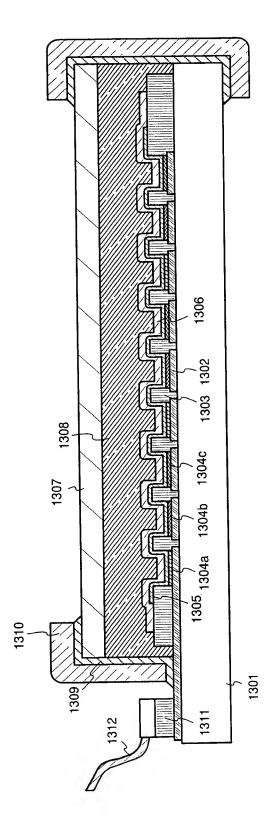
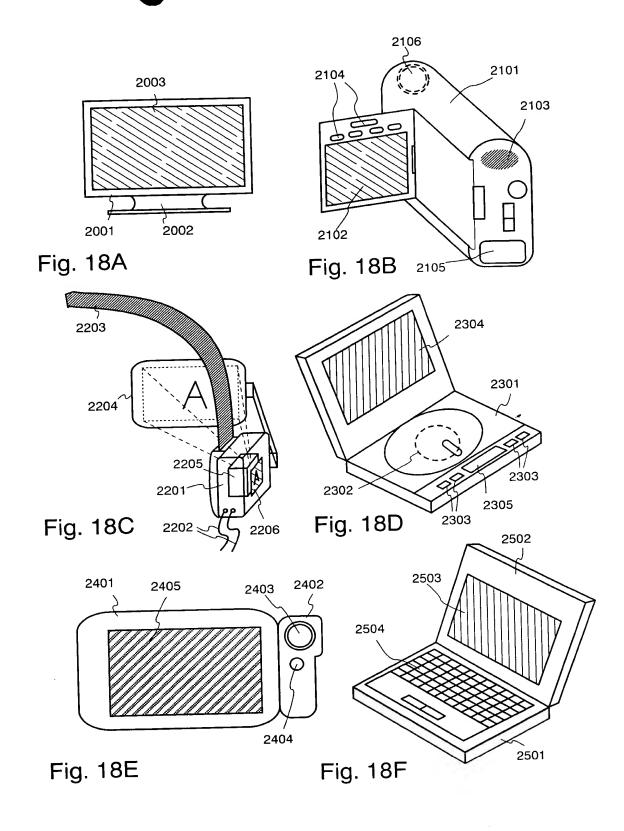
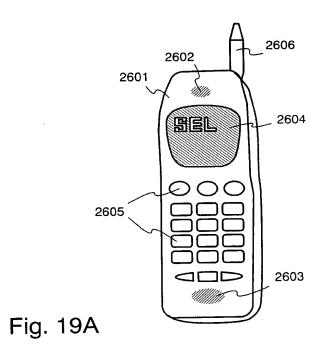


Fig. 17





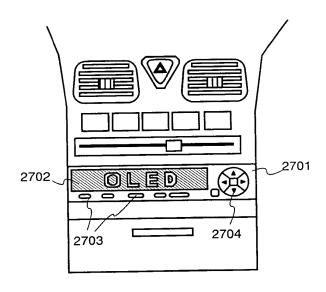
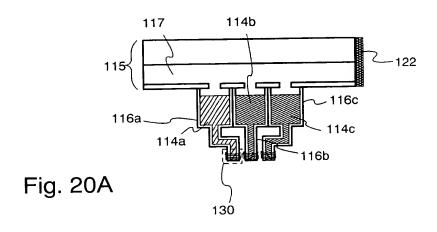


Fig. 19B



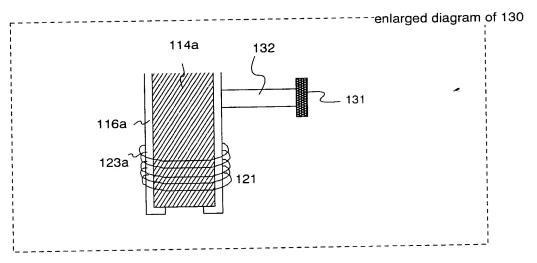


Fig. 20B